On page 1, line 8 please replace "higher" with --high--.

The following is a replacement paragraph:

--The invention relates, in general, to semiconductor microelectronic sensors, and more particularly, to single crystal silicon sensors that include structures with diverse contours and high aspect ratio geometries.--

On page 9, line 26 please replace "is" with --which are--.

The following is a replacement paragraph:

--Moreover, since the processing techniques described below permit deep etching independent of crystallographic directions, the beam 76 and the seismic mass 78 can be formed in (100) silicon wafers which are suitable for fabrication of MOS circuits. Hence, a MOS circuit can be readily formed in the upper face 82 of the seismic mass using standard semiconductor processing techniques.--

On page 12, line 31 please replace "experience" with--experienced--.

The following is a replacement paragraph:

--In operation, the short sense-beam will flex in a direction indicated by arrow 126'. The collection of interdigitated plates 130 and 132 will either experience an increase in overlap capacity or a decrease in overlap capacity depending upon the direction of deflection of the sense-beam 126. Thus, the capacitive plates can be used to sense a degree of deflection of the sense-beam. Alternatively, the interdigitated beams can be used to apply an electrostatic force sufficient to overcome the deflection of the beam. The degree of electrostatic force necessary to overcome such deflection is related to the acceleration experienced by the accelerometer 120. The circuitry used to determine the amount of flexure of the sense-beam, and the amount of overlap of the interdigitated plates 130 and 132 or, alternatively, to apply a countervailing electrostatic force, employ techniques well known to those skilled in the art and that are not part of the present invention. Hence they need not be described herein.--

On page 17, line 14, replace the "," after the initial "P" with a ".".

On page 17, line 19 after "region" please insert--)--.

The following is a replacement paragraph:

--In Figure 8F, the first wafer is patterned for a Deep Reactive Ion Etching (DRIE) step which defines the regions of the "top" wafer to be etched. DRIE techniques have become increasingly well known. For example, refer to: V.A. Yunkin, D. Fischer, and E. Voges, "Highly Anisotrophic Selective Reactive Ion Etching of Deep Trenches in Silicon," Microelectronic Engineering, Vol. 23, 1994, at 373-376; C. Linder, T. Tschan, N.F. de Rooij, "Deep Dry Etching Techniques as a New IC Compatible Tool for Silicon Micromachining," Proceedings, Transducers '91, June 1991, at 524-527; C.D. Fund and J.R. Linkowski, "Deep Etching of Silicon Using Plasma," Proceedings of the Workshop on Micromachining and Micropackaging of Transducers, Nov. 7-8, 1984, at 159-164; and J.W. Bartha, J. Greeschner, M. Puech, and P. Maquin, "Low Temperature Etching of Si in High Density Plasma Using $SF_6/0_2$," Microelectronic Engineering, Vol. 27, 1995, at 453-456. Reactive Ion etch equipment now allows the etching of holes or trenches which are very deep (>100 microns), while maintaining high aspect ratios (the ratio between the depth of the etched region and the width of the etched region). It has been found that this equipment is capable of at least 20:1 aspect ratios for trenches as deep as 300 microns.--

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On page 21, line 5, delete the second period "." in the sentence ending "214.".

On page 21, line 16, delete "si" and replace with "is".

On page 21, line 17, delete "recesses204" and replace with --recesses 204--.

The following is a replacement paragraph:

--In Figure 9B, a deep reactive ion etch (DRIE) process is employed to produce a high aspect ratio channel 216 which results in a suspended structure 218 surrounded by such high aspect ratio channel 216. The suspended structure 218 is suspended from the lower upstanding

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structure 212 which is attached to the lower wafer 214. The lower upstanding structure, therefore, anchors a lower end of the suspended structure 218 to the lower wafer 214. The channel 216, for example, can be circular which results in the formation of a generally cylindrical suspended structure 218. It will be appreciated, however, that a circular channel is just one of many possible channel shapes as explained below. Next, an upper wafer 220 is bonded to the wafer 200 enclosing the suspended structure 218 between the upper and lower wafers 220 and 214. The upper upstanding structure 210 has been etched so that its upper or distal end is below the upper surface of the middle wafer 200. As a result, when the uppper wafer 220 is bonded to the middle wafer 200, there is a gap between the upper upstanding structure 210 and the upper wafer 220. An upper or distal end of the suspended structure 218, is not unattached to the upper wafer 220 and is free to move about. The suspended structure 218 is disposed within a cavity defined by the etched recesses 204 and 206 and by the DRI etched channel 216. The lower upstanding structure 212 anchors the suspended structure 218 to the lower wafer 214 within the cavity. As illustrated in figures 1, 3, 6, 12A-12B and 13, the lower upstanding structure 212 can be constructed to be a flexible member, such as a spring or a beam, for sensor or actuator applications. Also, the suspended structure 218 may be encapsulated in an environment, gaseous or near vacuum, in which the bonding of the upper wafer 220 may take place.--

C6 cont.

On page 22, line 26 please replace " in," with --, in--.

The following is a replacement paragraph:

As an alternative to the overall fabrication process described above with respect to Figures 9A-9D, instead of forming recesses in a middle wafer, recesses could be formed in upper and lower (outer) wafers. For example, referring to the illustrative drawings of Figure 10, there is shown a side cross-sectional view of an alternative multiple wafer device with an SCS released structure 218". Upper and lower wafers 220' and 214' have recesses formed in them as shown. The recess in the upper wafer 220' and 214' have recesses formed in them as shown. The recess

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in the upper wafer 220' defines an upper upstanding structure 210'. The recess 206' in the lower wafer 214' defines a lower upstanding structure 212'. A middle wafer 200' that has a channel 216' formed by a deep reactive ion etch is bonded between the upper and lower wafers 214' and 220'. Thus, the released structure 218' is disposed within a cavity defined by the etched recesses 204' and 206' and by the DRI etch channel 216'. The actual process steps, in accordance with the invention, that produce the structure of Figure 10 will be appreciated by those of ordinary skill in the art from the explanation above relative to Figures 9A-9D and need not be set forth in detail herein.--

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On page 23, line 15 please replace " in," with --, in--.

The following is a replacement paragraph:

--Another alternative to the overall fabrication process described above involves the etching through both upper and lower wafers in order to release a structure formed from a middle wafer. Referring to the illustrative drawing of Figure 11, for example, there is shown a side cross-sectional view of another alternative multiple wafer device with an SCS released structure 218". The middle wafer 200" is etched in a manner similar to the wafer 200 of Figures 9A-9D. In particular, a channel 216" is formed by deep reactive ion etching. However, an upper upstanding structure 210" of the wafer 200" of Figure 11 is bonded to an upper wafer 200". Hence, in order to release the structure 218", a channel 222" is etched in a lower wafer 214", and a channel 228" is etched in the upper wafer 220". The actual process steps, in accordance with the invention, that produce the structure of Figure 11 will be appreciated by those of ordinary skill in the art from the explanation above relative to Figures 9A-9D and need not be set forth in detail herein.--

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On page 39, line 10 before "semiconductor" please insert --a--.

The following is a replacement paragraph: